IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTORS: Baruch SOLOMON, et al.

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TITLE: FILTERING BASIC INSTRUCTION SEGMENTS IN A PROCESSOR FRONT-END FOR POWER CONSERVATION

ART UNIT: 2189

EXAMINER: Zhuo H. LI

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

SIR:

The above-identified application having been finally rejected in the Office Action mailed April 29, 2005, this pre-appeal brief request for review is respectfully submitted.

Remarks/Arguments

Pursuant to 37 CFR § 1.116, cancellation of claims 21-24 without prejudice is requested. Accordingly, claims 1-20 are pending in the application. Claims 1-4 have been withdrawn from consideration pursuant to a restriction requirement by the Examiner. Claim 25 has been canceled by an earlier amendment. Of the remaining claims, claims 5-20 stand finally rejected.

The Examiner erred in rejecting claims 5-8 under 35 USC 102(e) as being anticipated by Yamashiroya (US 6,470,425).

Independent claim 5 is reproduced below:

5. A control method comprising, on a cache hit:

counting a number of accesses to a cache line that caused the hit,
if the count meets a predetermined threshold, enabling a segment builder,
building and storing instruction segments from an output of the segment builder.

The present invention relates to a power conservation method and system for processors. Implementing and managing instruction segments in a processor typically consumes much power. The present invention involves avoiding the costly implementation and managing of instruction segments when the instruction segments are not likely to be re-used. Accordingly, as recited in claim 1, instruction segments are only built and stored when a predetermined number of accesses to a cache line that caused a hit is counted, ensuring that the instruction segments are likely to be re-used and therefore the power expended in building and storing the instruction segments will not be wasted.

Yamashiroya is completely silent regarding building and storing instruction segments from an output of a segment builder, as required by claim 5. In the Advisory Action mailed 7/28/05, the Examiner equates the hit threshold register 461 of Yamashiroya with the latter claim feature. This is in error. Yamashiroya relates to a circuit for inhibiting data in a cache memory that is frequently accessed from being replaced. To this end, the circuit has counters whose values determine whether or not to protect cache entries from being overwritten. The hit threshold register counter 461 is one of these. See col. 3, line 66 to col. 4, line 6:

> "The hit threshold register 461 contains the number of sequential cache hits that is used as an update inhibition condition for a cache memory entry. That is, when the number of sequential cache hits on an entry exceeds the number of times specified in the hit threshold register 461, the update of the entry is inhibited thereafter."

However, there is absolutely no mention in Yamashiroya of claim 5's building and storing of instruction segments, either in connection with the hit threshold register 461 or in any other way. In the Advisory Action, the Examiner nevertheless concludes that Yamashiroya does in fact disclose building and storing of instruction segments, stating:

"... thereby the threshold register in combination with the inhibition information memory functioning the step of building and storing instruction segments from an output of a segment builder, i.e., updating of the cache entry in the inhibition information memory from the cache memory based on the number of sequential contained in the hit threshold register."

[Sic.] (Advisory Action, page 2, lines 6-9). This conclusion is not only completely unwarranted from the reference, which as previously noted is utterly silent as to building and storing instruction segments, but is illogical as well: inhibiting a cache entry from being overwritten, as in Yamashiroya, has nothing at all to with building and storing instruction segments as recited in claim 5. Claim 5, and claims 6-8 dependent thereon, are therefore allowable over Yamashiroya.

The Examiner erred in rejecting claims 9 and 10 under 35 USC 103(a) as being unpatentable over Yamashiroya in view of Chauvel et al. (US 6,681,297) ("Chauvel")

Claims 9 and 10 depend on claim 5 and therefore incorporate its limitations. Claim 5 has been demonstrated to be allowable over Yamashiroya as discussed above. Chauvel does not remedy the deficiencies in Yamashiroya with respect to claim 5, for at least the reason that Chauvel also does not disclose or suggest building and storing instruction segments as recited. Claims 9 and 10 are therefore allowable over Yamashiroya and Chauvel for at least the reasons discussed in connection with claim 5.

The Examiner erred in rejecting claims 11-25 under 35 USC 103(a) as being unpatentable over Miyazaki (US 6,385,697) in view of Chauvel.

Independent claim 11 is reproduced below:

11. An instruction cache, comprising:
an address decoder;
a plurality of cache entries, each indexed by an output of the address decoder and comprising a tag field, a count field and a data field;
an incrementor coupled to the access count fields; and
a threshold comparator coupled to the incrementor.

Claim 11 relates to an embodiment as shown in FIG. 5. The count field of each cache entry count accesses to the corresponding entry. An incrementor stores the counts. A threshold comparator coupled to the incrementor compares count values to a threshold, and if the threshold is met or exceeded, outputs an enable signal to an instruction segment builder.

Miyazaki does not suggest the claimed structure. Miyazaki relates to a cache system purported to achieve high speed data access and high cache hit rate by coupling full-set associative cache memory and non-full-set associative cache memory. Among features of claim 11 absent from Miyazaki is a threshold comparator coupled to an incrementor coupled to access count fields. Element 32 of Miyazaki, alleged by the Examiner to be equivalent to the claimed threshold comparator, is instead an OR gate coupled to two AND gates respectively coupled to a full-set associative cache and a non-full-set associative cache, and associated comparators. The OR gate 32 indicates whether a hit or a miss occurred in either a cache line of the full-set associative cache or the non-full-set associative cache. If a hit occurs in either, data from the hit cache line is sent to an instruction decoder. See Miyazaki at col. 14, lines 42-55, and FIG. 5. Thus, OR gate 32 is neither coupled to an incrementor coupled to access count fields, nor is it a threshold comparator, as by contrast is recited in claim 11. Chauvel does not remedy the deficiencies in Miyazaki.

Independent claim 16 recites an embodiment wherein a threshold comparator is coupled to count fields, and an incrementor is coupled to the threshold comparator. Along lines discussed above, Miyazaki and Chauvel do not suggest the claimed structure.

In view of the above, independent claims 11 and 16 are allowable over Miyazaki and Chauvel. Moreover, since they include the recitations of one of claims 11 or 16 by dependency thereon, claims 12-15 and 17-20 are similarly allowable over Miyazaki and Chauvel, for at least the reasons discussed in connection with claims 11 and 16.

Conclusion:

In view of the above, the Applicant respectfully submits that the claims of the present application are allowable over the art of record. The Applicant therefore respectfully requests that the review panel allow the claims.

The Examiner is invited to contact the undersigned at (202) 220-4323 to discuss any matter concerning this application. The Office is authorized to charge any fees related to this communication to Deposit Account No. 11-0600.

Respectfully submitted,

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